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integrated circuit and thereby still forming part of the package. The debug interface can communicate with the debug support circuits either using dedicated on-chip interconnects, or by using the system interconnect. The system interconnect can be a conventional bus of hierarchy of busses, or a network on-chip or other in-package network. The high speed debug
5 interface can include additional circuits to use a packet switched network for the efficient movement of debug support data.

Various modifications will be apparent to those skilled in the art.

CLAIMS

1. An integrated circuit assembly for use in a system, comprising:
a first arrangement of connection terminals for connecting the integrated circuit to
5 other components of the system;
debug circuitry;
a debug interface comprising a second arrangement of connection terminals;
a signal conversion arrangement coupled to the second arrangement of connection
terminals for converting electrical signals provided to the second arrangement of terminals
10 into a format for transmission to external monitoring circuitry; and
a communications link for communicating the data provided to the second arrangement
of terminals to the external monitoring circuitry.
2. An assembly as claimed in claim 1, wherein the signal conversion arrangement
15 comprises electro-optical conversion means, and the communications link comprises an
optical communications link.
3. An assembly as claimed in claim 2, wherein the electro-optical conversion means
comprises an array of lasers.
- 20 4. An assembly as claimed in claim 3, wherein the lasers comprise vertical cavity surface
emitting lasers.
5. An assembly as claimed in claim 1, wherein the signal conversion arrangement
25 comprises analogue electrical circuitry for implementing digital communication over the
communications link.
6. An assembly as claimed in claim 1, wherein the signal conversion arrangement
comprises analogue electrical circuitry for providing a control signal for controlling an electro-
30 optical conversion means.

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7. An assembly as claimed in any preceding claim, wherein the first arrangement of connection terminals are provided as a ring of terminals around the periphery of an upper surface of the assembly, and the second arrangement of connection terminals are provided on the upper surface of the assembly within the ring.

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8. An assembly as claimed in claim 7, wherein the second arrangement of terminals are formed from a top metal layer of the assembly.

9. An assembly as claimed in any one of claims 1 to 6, wherein the first and second arrangements of connection terminals together define a ring of terminals around the periphery of an upper surface of the assembly.

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10. An assembly as claimed in any preceding claim, further comprising a second integrated circuit memory device, comprising a third arrangement of connection terminals connected to the first or second arrangement of connection terminals of the first integrated circuit, wherein the debug interface provides access to internal operation information of the first and second integrated circuits.

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11. A set of integrated circuits, comprising
at least one first integrated circuit assembly having debug capability and as claimed in any preceding claim; and

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a plurality of second integrated circuit assemblies having the same design as the at least one first assembly in respect of the first arrangement of connection terminals and the debug interface, and wherein the plurality of second assemblies are not provided with the communications link of the at least one first assembly.

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12. A set as claimed in claim 11, wherein the plurality of second integrated circuit assemblies have the same design as the at least one first assembly in respect of the debug circuitry, and wherein the plurality of second assemblies are also not provided with the signal conversion arrangement of the at least one first assembly.

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13. A method of performing a debug operation, using an integrated circuit assembly comprising a first arrangement of connection terminals, debug circuitry, and a debug interface comprising a second arrangement of connection terminals, the method comprising:

coupling a signal conversion arrangement to the second arrangement of connection
5 terminals;

using the signal conversion arrangement to convert electrical signals provided to the second arrangement of terminals into a second format;

transmitting the signals using the second format to external monitoring circuitry; and

performing a debug operation using the external monitoring circuitry.

10 14. A method as claimed in claim 13, wherein the second format comprises an optical transmission format and the signal conversion arrangement comprises electro-optical conversion means.

15 15. A method as claimed in claim 14, wherein the electro-optical conversion means comprises an array of lasers.

16. A method as claimed in claim 15, wherein the lasers comprise vertical cavity surface emitting lasers.

20 17. A method as claimed in claim 13, wherein the second format comprises a signal format for controlling an electro-optical conversion means.

18. An integrated circuit assembly for use in a system, comprising:

25 a first integrated circuit, comprising:

a first arrangement of connection terminals for connecting the integrated circuit to other components of the system;

debug circuitry;

a debug interface comprising a second arrangement of connection terminals;

30 and

a second integrated circuit memory device, comprising:

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a third arrangement of connection terminals connected to the first or second arrangement of connection terminals of the first integrated circuit,

wherein the debug interface provides access to internal operation information of the first and second integrated circuits.

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19. An assembly as claimed in claim 18, wherein the first integrated circuit further comprises a signal conversion arrangement coupled to the second arrangement of connection terminals for converting electrical signals provided to the second arrangement of terminals into a format for transmission to external monitoring circuitry, and a communications link for communicating the data provided to the second arrangement of terminals to the external monitoring circuitry.

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20. An assembly as claimed in claim 18, wherein the first integrated circuit further comprises a signal conversion arrangement coupled to the second arrangement of connection terminals for converting electrical signals provided to the second arrangement of terminals into a format for controlling an electro-optical conversion means for transmission to external monitoring circuitry, and an optical communications link for communicating the data provided to the second arrangement of terminals to the external monitoring circuitry.

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